Improved Electrical and Thermal Performance of Ultra-thin RF LDMOS Power Transistors

J.A. Herbsommer, H. Safar, W.Brown, E.W. Lau, D.P. Farrell, P.Gammel ,O.Lopez, and G. Terefenko

Agere Systems, 700 Mountain Ave. Murray Hill NJ 07974, USA.

Abstract — **We present the electrical and thermal performance of ultra-thin RF LDMOS devices. Following a proprietary process, we fabricated such devices with a thickness as reduced as 40μm. This results in a reduction of the operating junction temperature, as demonstrated by infrared imaging experiments and three-dimensional finite-element-analysis simulations. As a result, the thermal resistance of our packaged devices reaches substantially lower values than industry standard. This allows for a higher power output and improved efficiency, as demonstrated by RF measurements.**

I. INTRODUCTION

Due to the rather poor thermal conductivity of silicon, and impact on parasitics, die thickness plays an important role on the performance of many electronic devices [1]. In the case of power devices die thickness limits the thermal performance due to junction heating (as discussed, for example, by Lindsted and Surty [2]). In cases where contact to ground is made through the die, the die thickness can determine both RF efficiency of the device and device parasitics. With the purpose of improving these aspects of power devices we have developed a high yield process to fabricate ultra-thin RF LDMOS transistors, down to 40 μm die thickness. In this paper we analyze the thermal and electrical the advantages of these ultra-thin dies and measure their impact in RF LDMOS technology. We demonstrate that ultra-thin dies operate at a substantially reduced junction temperature, reaching a junction-to-case thermal resistance significantly lower than current industry standards. Electrically, this reduced junction temperature allows for higher output power and efficiency, as we demonstrate by DC IV and RF measurements. Compared to 150μm thick dies, our 40μm ultra-thin RF LDMOS devices reach 14% higher maximum power output (P1dB) and 9% higher drain efficiency.

II. THERMAL RESISTANCE OF ULTRA-THIN DIES

Shown in Fig. 1 is a 127mm wafer containing our LDMOS devices (with an approximate die size of 1mm x 5mm). This wafer was thinned following our proprietary process, which can controllably produce devices as thin as 40 μm. The diced wafer in the picture is 40 μm thick, and the devices are ready to pick and package. The yield for process approaches 100%. It can also be inferred from the picture in Fig. 1 that both wafer fragility and bow have been minimized in our thinning process.

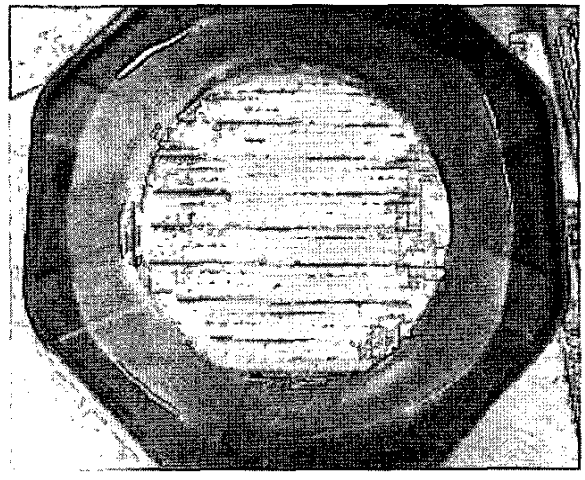

Fig. 1. Wafer (127mm diameter) thinned to 40μm already diced. The ultra-thin LDMOS devices are ready for assembly

Normally these devices are housed in CuW packages, that are attached to a thermal sink for operation. A typical device dissipate in the order of 600W/cm^2, leading to a substantial junction heating. A large fraction of the junction to case thermal resistance of packaged devices comes from the temperature gradient across the die itself [2]. This is because the low thermal conductivity of silicon and the reduced die area that restricts heat flow. This can be directly measured using infrared (IR) imaging techniques (Fig. 2) as well as simulated (Fig. 3) using accurate 3D finite-element analysis models that take into account the exact gate finger distribution across the device.

0-7803-7695-1/03/$17.00 © 2003 IEEE

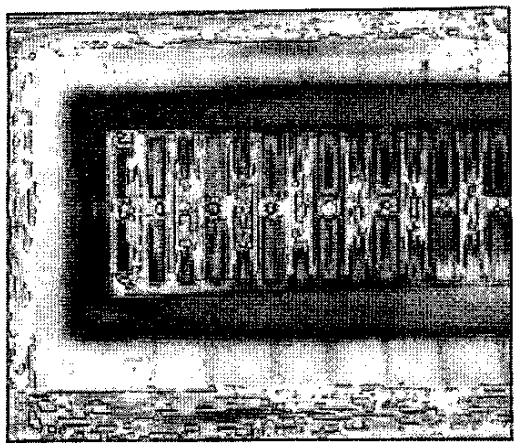

Fig.2 Junction temperature of devices in operation (Pdiss=30W) is directly measured by infrared imaging.

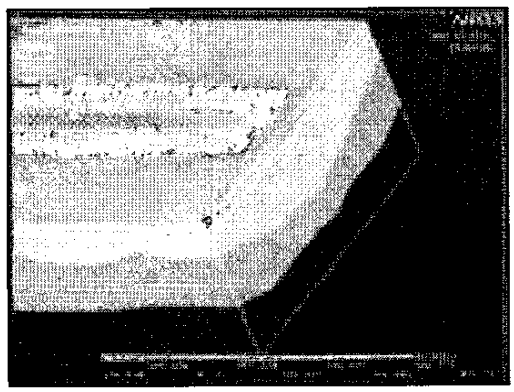

Fig. 3. Realistic 3D-FEA simulations are used to calculate device heating from a macroscopic to a single-gate finger scale.

As shown in Fig 4, infrared imaging measurements reveal a substantial reduction of the junction temperature for the ultra-thin die. This results in a 2x reduction of the junction-to-case thermal resistance, as shown in Fig. 5. It is interesting to note that the package contribution to the thermal resistance is relatively small for thick dies, while becomes important for ultra-thin dies, calling for the need of better packaging materials.

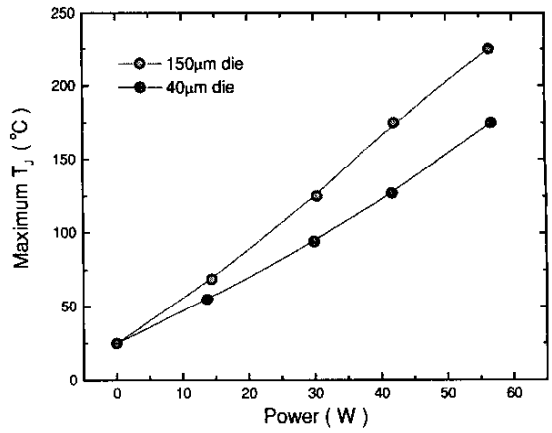

Fig. 4. Shown is the maximum junction temperature measured in IR experiments vs. dissipated power for devices made with different die thickness.

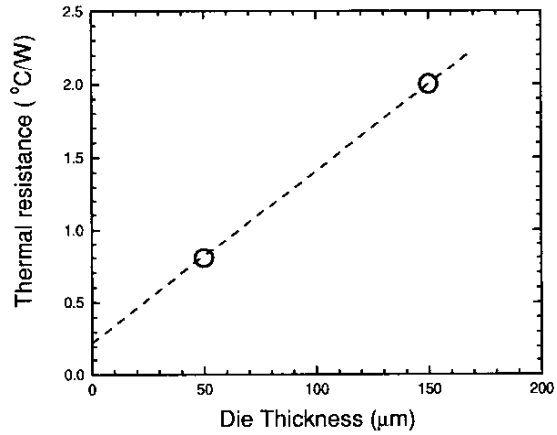

Fig. 5. Junction-to-Case thermal resistance vs die thickness for single-die devices in CuW packages. The extrapolation to zero die thickness indicates the package's thermal resistance.

The effect of the junction temperature on IV curves is shown in Fig. 6. A noticeable higher knee region is found at lower junction temperature. By means of a load-line analysis assuming class AB operation, the power output is calculated from the IV curves, and plotted in Fig. 7. Also shown in Fig. 7 is the power output vs. junction temperature measured in RF CW experiments at 895MHz. .

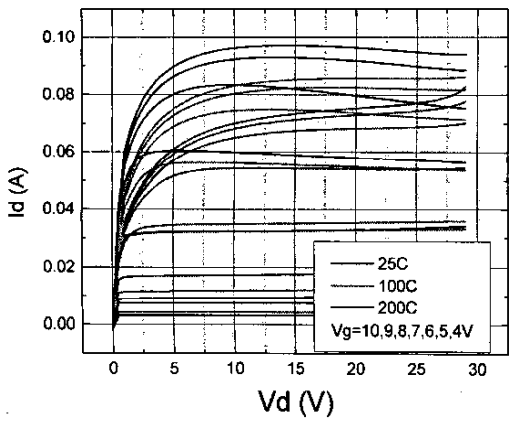

Fig. 6 DC IV curves measured on 0.6mm gate width test structure for different junction temperatures.

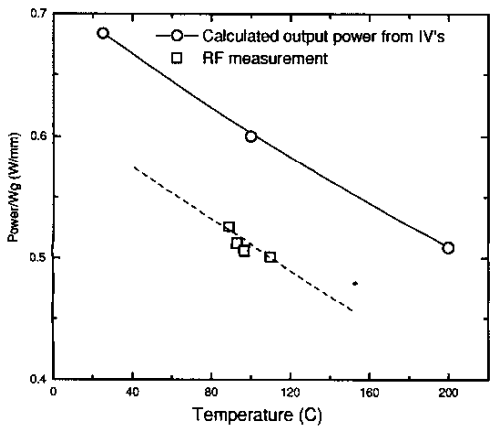

Fig. 7 Normalized power per total gate width vs. junction temperature, ○: as calculated from IV curves (see Fig. 6). ❑ measured in CW 895MHz experiments on a 120mm total gate width device.

There is good agreement of the absolute value and trend with junction temperature for both DC and RF output power determinations

We also conducted narrowband CW experiments at 895Mhz on devices using 40μm dies, and compared to identical measurements on devices using 150μm dies. In both cases, case temperature was kept near 100C, thus the 40μm dies will operate at a reduced junction temperature. Shown in Fig. 8 is gain vs. power out plot of devices using 150 and 40μm thick dies.

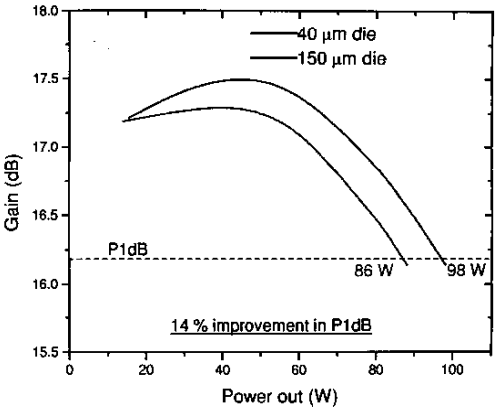

Fig.8 Gain vs output power for devices of different die thickness. A higher power output (defined at the 1dB gain compression point) is measured in devices made of ultra - thin dies.

For this experiment, the setup was optimized for maximum power output for each device. The device using ultra-thin dies reaches a 14% higher power output, defined at the 1dB gain compression point. Under the same experimental conditions we observe an improved drain efficiency of devices with ultra-thin dies, as shown in Fig 9 by the plot of drain efficiency vs. output power.

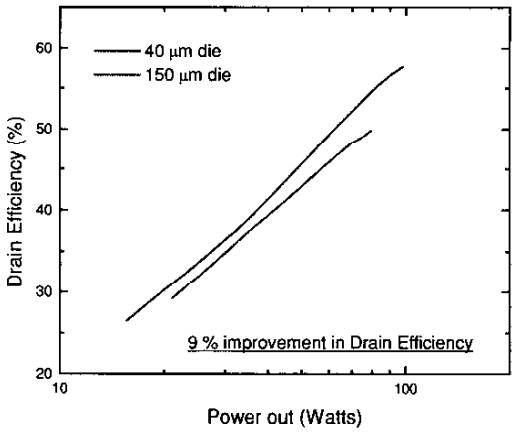

Fig.9 Drain efficiency vs. output power for devices of different die thickness. A substantially improved efficiency is measured in devices made of ultra-thin dies

The above results illustrated the advantages of ultra-thin dies from a device perspective. We want to mention that there are also other advantages that are realized from a

system level perspective. An important improvement, for example, is the expected longer mean time to failure (MTTF) rate of these devices due to their cooler operating temperatures. Due to the thermally activated nature of the failure processes (see for example Black [3]), a two fold increase in MTTF can be expected, resulting in a reduced failure rate of a given ensemble of devices over their operating life.

III. CONCLUSIONS

We demonstrated the thermal and electrical superior performance of ultra-thin RF LDMOS power transistors. We have shown that these devices have a smaller junction to case thermal resistance in comparison to regular thickness dies. This improvement results in a substantially lower junction temperature. As shown by dc IV and RF measurements, a reduced junction temperature allows for an increased power output and higher drain efficiency.

ACKNOWLEDGEMENT

We acknowledge and thank R. H. Shanaman, S. M. Hawkin, D. J. Gaydos and P. F. Leyman for their contributions in developing a manufacture worthy wafer thinning process.

REFERENCES

[1] S.M. Sze, Physics of Semiconductor Devices, John Wiley & Sons, New York 1981

[2] R.D. Lindsted and R.J. Surty "Steady-State Junction Temperatures of Semiconductor Chips", IEEE Trans. Electron Devices, vol ED-19 No 1, pp. 41-44, January 1972

[3] J. Black, "Electromigration failure modes in aluminum metallizations for semiconductor devices," Proc. IEEE , vol. 57, pp. 1587-1631, March 1969